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A SURVEY ON DESIGN AN EFFICIENT ARCHITECTURE FOR HIGH SPEED CONVOLUTION AND DECONVOLUTION PROCESS

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ABSTRACT
In Digital Signal Processing, the convolution and deconvolution with a very long sequence is ubiquitous in many application areas. They consume much of time. This paper presents a direct method of computing the discrete linear convolution, circular convolution and deconvolution. The most significant aspect, is the development of a multiplier and divider architecture based on high speed algorithm. It shows that the implementation of linear convolution and circular convolution is efficient in terms of area and speed compared to their implementation using conventional multiplier & divider architectures. In this paper we study different forms of high speed convolution and deconvolution system using FPGA.

INTRODUCTION
Convolution and deconvolution is the most important and fundamental concept in signal processing and analysis. However, beginners often struggle with convolution and decovolution because the concept and computation requires a number of steps that are tedious and slow to perform. Therefore many of researchers have been trying to improve performance parameters of convolution and deconvolution system using new algorithms and hardware. Complexity and excess time consumption are always the major concern of engineers which motivates them to focus on more advance and simpler techniques. Pierre and John have implemented a fast method for computing linear convolution, circular convolution and deconvolution .This method is similar to the multiplication of two decimal numbers and this similarity makes this method easy to learn and quick to compute. Also to compute deconvolution of two finite length sequences, a novel method is used. This method is similar to computing long-hand division and polynomial division .Following diagram shows the overall process of high speed convolution and deconvolution process. With the latest advancement of VLSI technology, digital signal processing plays a pivotal role in many areas of electrical engineering. of Digital Signal Processing and Image Processing. It is used for designing of digital filter and correlation application. However, beginners often struggle with convolution because the concept and computation requires a number of steps that are tedious and slow to perform. Discrete convolution is central to many applications. The most commonly taught approach is a graphical method because of the visual insight into the convolution mechanism. Graphical convolution is very systematic to compute but is also very tedious and time consuming. The principal components required for implementation of convolution calculation are adder and multiplier for partial multiplication. Therefore the partial multiplication and addition are bottleneck in deciding the overall speed of the convolution implementation technique. Complexity and excess time consumption are always the major concern of engineers which motivates them to focus on more advance and simpler techniques.

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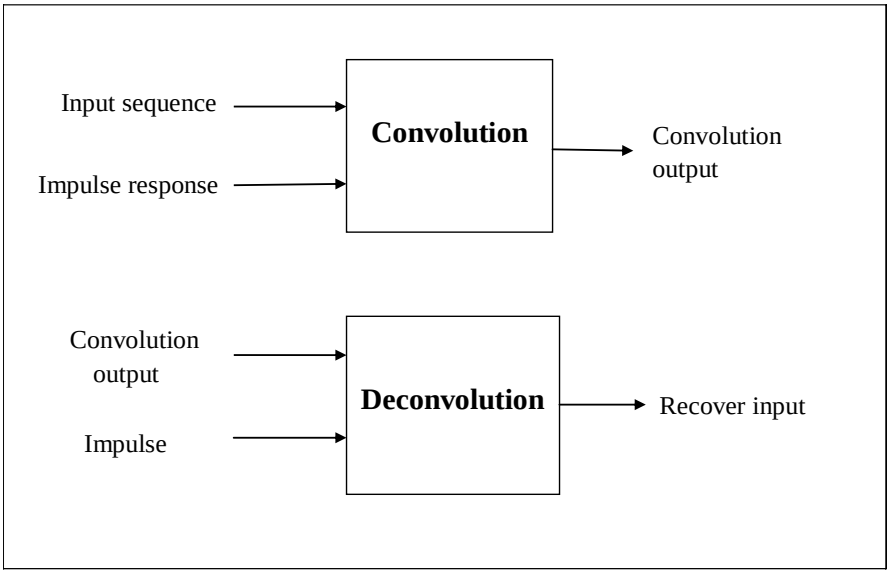

Fig 1.Block diagram of Convolution and Deconvolution process

LITERATURE REVIEW

Surabhi Jain & Sandeep Saini [1] presents a direct method of computing the discrete linear convolution, circular convolution and deconvolution. The approach is easy to learn because of the similarities to computing the multiplication of two numbers. The most significant aspect of the proposed method is the development of a multiplier and divider architecture based on Ancient Indian Vedic Mathematics sutras Urdhvatriyagbhyam and Nikhilam algorithm. The results show that the implementation of linear convolution and circular convolution using vedic mathematics is efficient in terms of area and speed compared to their implementation using conventional multiplier & divider architectures.

G.Ramanjaneya Reddy, A. Srinivasulu [2] presents an on the spot methodology of reducing convolution processing time using hardware computing and implementations of discrete linear convolution of two finite length sequences (NXN). This implementation method isrealized by simplifying the convolution building blocks. The purpose of this analysis is to prove the feasibility of an FPGAthat performs a convolution on an acquired image in real time. . In addition, the presented circuit uses less power consumption and delay from input to output. It additionally provides the required modularity, expandability, and regularity to form different convolutions for any variety of bits.-+.

Sukhmeet Kaur, Suman and Manpreet Signh Manna [3] describes implementation of radix-4 Modified Booth Multiplier and this implementation is compared with Radix-2 Booth Multiplier. Modified Booth's algorithm employs both addition and subtraction and also treats positive and negative operands uniformly .No special actions are required for negative numbers. The Speed and Circuit Complexity is compared, Radix-4 Booth Multiplier is giving higher speed as compared to Radix-2 Booth Multiplier and Circuit Complexity is also less as compared to it.
Madhura Tilak [4] presents a novel method of implementing linear convolution of two proposed method uses modified design approach by replacing the conventional multiplier by Vedic multiplier internally in the implementations. The proposed method is efficient in terms of computational speed, hardware resources and area significantly. The efficiency of the proposed algorithm is tested by simulations and comparisons with different design approaches.The proposed circuit is also modular, expandable and regular which provides flexibility

Rashmi Lomte [6] describes a methof of two finite length sequences (NXM), is implemented using direct method to reduce deconvolution processing time.The perfomance of the circuit has a delay of 79.595 ns from input to output using 90nm process.The outcome of research is high speed deconvolver implementation is achieved. Since 4×4 bitmultiplier is need of this project, different 4×4 bit multipliersare studied and Urdhava Triyakbhyam algorithm which gives lowest delay among remaining all multipliers is used .

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PROPOSED WORK

Convolution is an important mathematical tool in both fields of signal and image processing. It is employed in filtering , denoising,edge detection, correlation, compression, deconvolution,simulation, and in many other applications Deconvolution is a computationally intensive digital signal processing (DSP) function widely used in applications such as imaging, wireless communication, and seismology.

The linear convolution is a basic operation in DSP which relates input signal and impulse response to obtain desired output. Consider two finite length sequences f(n) and g(n) on which the convolution operation is to be performed with lengths l and m respectively. the output of convolution operation y(n) contains l+m-1 number of samples. The formula for calculating discrete linear convolution is,

$$y(n) = \sum_{k=-\infty}^{\infty} x(k)h(n-k)$$

The concept of deconvolution is also widely used in the techniques of signal processing and image processing.In general, the object of deconvolution is to find the solution of a convolution equation of the form:

$$f * g = h$$

Usually, *h* is some recorded signal, and *f* is some signalthat wish to recover, but has been convolved with someother signal *g* before get recorded. The function *g* mightrepresent the transfer function of an instrument or a drivingforce that was applied to a physical system.If one know g or at least form of g,then one can perform deterministicdeconvolution. Convolution is the mathematical process that relates the output, y(t), of a linear, time-invariant system to its input, x(t), and impulse response, h(t). The overlap-add method (OLA) is an efficient way to evaluate the discrete convolution between a very long signal x[n] with a finite impulse response. h[n]**.**The Fig.1 shows the concept of overlap add method by Zero-pad length-*L* blocks by *M*−1 samples. Add successive blocks, overlapped by *M*−1 samples, so that the tails sum to produce the complete linear convolution. The Block Diagram of proposed sysyetm is,

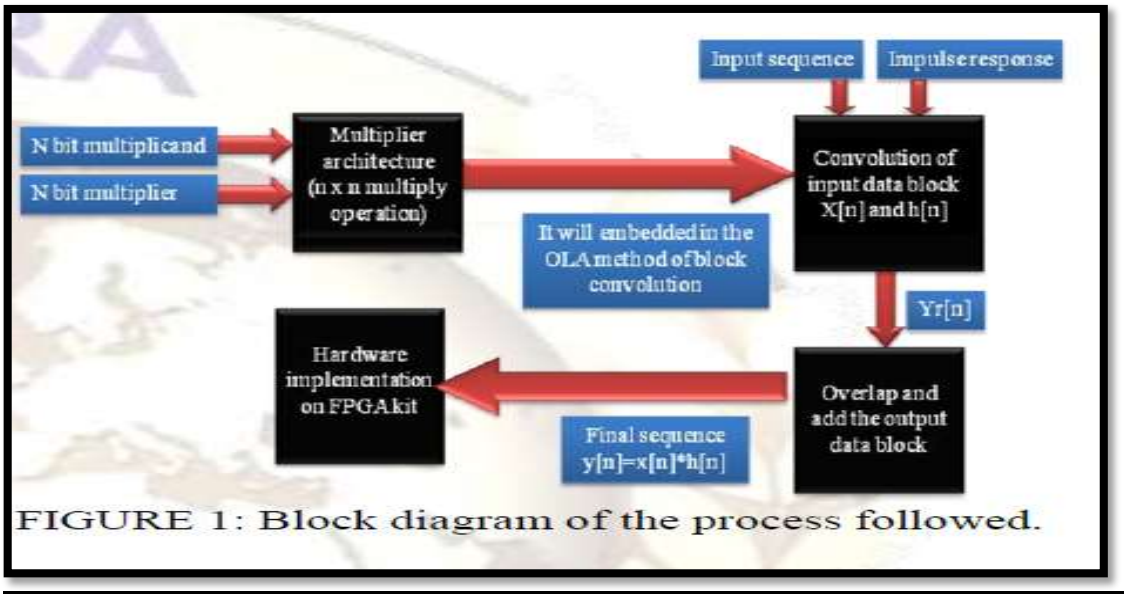

FIGURE 1: Block diagram of the process followed.

CONCLUSION

The main focus of this paper is to introduce a method for calculating the linear convolution, circular convolution and deconvolution with the help of vedic algorithms that is easy to learn and perform. An extension of the proposed linear convolution approach to circular convolution using vedic multiplier is also introduced which has less delay and area than the conventional

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method. This paper also introduced a straightforward approach to performing the deconvolution . The Vedic Methods enable the practitioner improve mental abilities to solve difficult problems with high speed and accuracy. Radix-4 Booth Multiplier is giving higher speed as compared to Radix-2 Booth Multiplier and Circuit Complexity is also less as compared to it.

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